IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellant:	Birdsley et al.	Examiner:	Wille, D.
Serial No.:	09/755,008	Group Art Unit:	2814
Filed:	January 5, 2001	Docket No.:	AMDA.469PA
Title:	Optical Analysis of Integrated Circuits		

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence and the papers, as described hereinabove, are being deposited in the United States Postal Service, as first class mail, in an envelope addressed to: Board of Patent Appeals and Interferences, United States Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450, on September 22, 2004.

By: Erin M. Nichols
Erin M. Nichols

APPEAL BRIEF

Board of Patent Appeals and Interferences
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is an Appeal Brief submitted pursuant to 37 C.F.R. § 41.37 for the above-referenced patent application. Please charge Deposit Account No. 01-365 (TT3943) in the amount of $330 for this brief in support of appeal as indicated in 37 C.F.R. § 41.20(b)(2). If necessary, authority is given to charge/credit deposit account 01-365 (TT3943) any additional fees/overages in support of this filing.

I. Real Party in Interest

The real party in interest is Advanced Micro Devices, Inc., having a place of business at One AMD Place, P.O. Box 3453, Sunnyvale, California. This application is assigned to Advanced Micro Devices, Inc.

II. Related Appeals and Interferences

Appellant is unaware of any related appeals, interferences or judicial proceedings.

III. Status of Claims

Claims 1-11 have been canceled and claims 12-20 are rejected. Claims 12-20 are presented for appeal and may be found in the attached Appendix of Appealed Claims in their present form.

IV. Status of Amendments

The Office Action and Amendment After Final filed on June 28, 2004, included the cancellation of claims 1-11 (non-elected claims). The Advisory Action dated July 20, 2004, indicated that the amendment would be entered.

V. Summary of Invention

One embodiment of Appellant's invention is directed to an arrangement for analyzing an integrated circuit having a silicon on insulator (SOI) structure 15. The arrangement includes a means for directing a modulated optical beam 120 at a selected portion of the SOI structure where the modulation is adapted to inhibit optical beam intrusion upon the integrated circuit and means for obtaining a reflected optical waveform response (*e.g.*, Fig 3) from the SOI selected portion. The means for directing may include, for example an IR laser as discussed at page 8, line 15 – page 9, line 15, and the means for obtaining a reflected optical waveform response may include, for example, a computer arrangement 150, as discussed at page 10, lines 1-10.[1]

Other embodiments are directed to using a combination of an optical beam arrangement 110 and a detection arrangement 140 to formulate the system of the present invention.

[1] Appellant notes that the two means limitations may optionally be implemented using the same tool. A single structural element may perform two functions and may support two different claim terms. *Reed v. Edwards,* 26 C.C.P.A. 901, 101 F.2d 550, 554, 40 USPQ 620, 622 (CCPA 1939); *In re Kelley,* 49 C.C.P.A. 1359, 305 F.2d 909, 914, 134 USPQ 397, 401 (CCPA 1962) (as cited in the unpublished decision of *Winbond Elec. Corp. v. Int'l. Trade Comm.*, 4 Fed.Appx. 832, 2001 WL80412 (Fed. Cir. Jan. 13, 2001)).

VI. Grounds of Rejection

Appellant has attempted to comply with new rule 37 C.F.R. § 41.37(c) by providing the Office Action's grounds of rejection verbatim, followed by an argument section corresponding thereto.

A. Claims 12-20 are rejected under 35 U.S.C. § 112(2).

B. Claims 12[-20] are rejected under 35 U.S.C. § 103(a) over Paniccia et al. (U.S. Patent No. 6,072,179) in view of Kikuchi (U.S. Patent No. 5,999,006).

VII. Argument

A. The Examiner's continued rejection of claims 12-20 under 35 U.S.C. § 112(2) improperly ignores the evidence of record.

Appellant has repeatedly explained that the sole evidence of record, including dictionary definitions, supports the plain meaning of the rejected claim terms. These terms concern the modulation of an optical beam being adapted to "inhibit optical beam intrusion upon the integrated circuit." The MPEP requires that claim terms be read in view of their plain meaning when used in a manner consistent with the accepted meaning. *See* MPEP § 706.03(d). This questioned claim terminology was explained in both the Office Action Response filed on February 19, 2004, and in the Office Action Response and Amendment After Final filed on June 28, 2004. The Examiner is incorrect in suggesting that the term "inhibit" can be interpreted to also be limited to the extreme condition of preventing the optical beam from reaching the circuit. As supported by the instant Specification, *e.g.*, page 6, lines 14-20, and Figure 1, the modulated optical beam reaches the selected portion of the die and the laser modulation is used to inhibit the optical beam's intrusion on the IC:

> According to an example embodiment of the present invention, an optical beam is directed at a selected portion of a conventional flip chip type SOI die. The beam is pulsed at an interval that is sufficient to inhibit intrusion of the beam into the die. A reflected optical response from the SOI is obtained from the die and used to generate a waveform representing an electrical characteristic of the die. In this manner, analysis of SOI flip chip dies is made possible while maintaining minimal beam intrusion, and without necessarily destroying the die.

Also, the dictionary definition of "inhibit" is consistent with Appellant's Specification: the Merriam-Webster online dictionary (www.m-w.com) defines "inhibit" as to hold in check, or restrain and the dictionary at www.hyperdictionary.com defines "inhibit" as to limit the range or extent of. As Appellant has explained that the claim term at issue is directed to an optical beam of short duration so as to limit intrusion on the integrated circuit, the rejection is based on an unsupported and irrelevant comment or opinion proffered by the Examiner. Appellant also fails to recognize the import of the Examiner's argument that the Specification should have been clearer about this unsupported comment in the final Office Action dated April 27, 2004. It would appear, as further discussed below, that the Examiner is attempting to ignore important claim limitations in order to support the stated prior art rejection. Appellant submits that the Examiner has ignored the evidence of record; and therefore, the Section 112(2) rejection is improper and should be withdrawn.

B. The rejection of claims 12[-20] is generally improper and the rejection of claim 15 is further deficient.

1. The rejection of claims 12[-20] is generally improper because the Examiner has failed to satisfy each of the three requirements of a *prima facie* Section 103(a) rejection.

The Examiner has failed to satisfy each of the three requirements of a proper Section 103(a) rejection. In order to present a proper Section 103(a) rejection, the Examiner must present a combination of references that teaches or suggests each of the claimed limitations, present evidence of suggestion or motivation to combine the cited references, and have a reasonable expectation of success for the proposed combination. MPEP § 2143. Throughout the prosecution of this application, Appellant has shown that the Examiner has failed to satisfy any of these three criteria; therefore, the Section 103(a) rejection is improper and should be withdrawn.

i. Cited References Fail to Correspond to the Claimed Invention

The Examiner has failed to identify a combination of references that corresponds to the claimed invention and, more specifically, has failed to present any teachings in the cited references of a modulated beam adapted to inhibit optical beam intrusion upon an integrated circuit. *See* independent claims 12 and 13. While the Examiner alleges that the '179 reference teaches the alleged mode-locked laser modulation being used to inhibit optical beam intrusion upon the integrated circuit, Appellant fails recognize where this teaching exists. The Examiner has not cited any teachings in the '179 reference that would correspond to these claimed limitations. The '006 reference fails to compensate for this deficiency in the '179 teachings, as the '006 light is not modulated nor modulated so as to inhibit optical beam intrusion, as claimed. Without a showing of complete correspondence to each of the claimed limitations, the Section 103(a) rejection is improper and cannot be maintained. Appellant accordingly requests that the rejection be withdrawn.

Moreover, it would appear that the Examiner is employing a Section 112(2) rejection in an attempt to ignore certain of Appellant's claim language. As discussed above, Appellant has provided both an explanation and support to further clarify the claim language at issue. Thus the Section 112 rejection is improper and should not be used as a shield to ignore certain claim limitations. Correspondence must be shown to each of the claim limitations to sustain a Section 103(a) rejection and the Examiner has failed to satisfy this requirement.

ii. No Evidence Has Been Provided to Combine the Cited References

The Examiner has failed to present evidence of motivation to combine the cited references to achieve the limitations of the present invention. The primary, '179, reference, as acknowledged by the Examiner, makes no mention of SOI structures. Therefore the '179 teachings fail to recognize problems associated specifically with SOI structures. The Examiner erroneously asserts that since the '006 reference teaches an optical technique for analyzing an SOI structure, "it would be obvious" to use the '179 optical technique for an SOI substrate because both SOI structures and the '179 substrates contain circuits. The optical techniques taught by the '179 and '006 references respectively are entirely different techniques that are not necessarily interchangeable to various devices and structures. The Examiner has not cited any teachings in the '179 reference that would suggest using the '179 optical techniques for SOI structures. Moreover, the Examiner fails to identify how the '179

teachings would be modified to address the specific problems associated with SOI structures, *e.g.*, optical beams disrupting or damaging circuitry components. Without a presentation of evidence from the cited teachings, that one skilled in the art would combine the cited teachings to achieve the limitations of the claimed invention, the Section 103(a) rejection is improper and should be withdrawn.

iii. Proposed Combination is Destructive, Undermining Any Expectation of Success

Further, the Examiner should not have an expectation of success because the proposed modification would frustrate the purpose and operation of the '179 teachings thereby rendering the proposed modification unmotivated and improper. The MPEP states that when a proposed modification would render the teachings being modified unsatisfactory for their intended purpose, there is no suggestion or motivation to make the proposed modification under 35 U.S.C. § 103(a). *See* MPEP § 2143.01. The Office Action suggests inserting the damaged '006 substrate (substrate has pin holes in the buried oxide layer as shown in Figures 1, 4 and 5) or the damaging analysis technique of the '006 teachings into the '179 teachings. The '179 reference is directed to operating a DUT to detect electrical waveforms corresponding to varying voltages. *See* col. 7, line 65 – col. 8, line 2. The damaged '006 substrate would not operate properly while under test to provide the desired voltage correlation data. Moreover, the '179 backside analysis technique would result in the mode-locked laser intruding into the SOI circuitry thereby disrupting the operation of the structure and likely damaging the circuitry, thus eliminating the possibility of testing the structure's integrity. To suggest that the skilled artisan would use the '179 teachings on the '006 SOI structure is untenable and would undermine the purpose and operation of the '179 reference. Thus, the proposed combination is unmotivated and Appellant requests that the Section 103(a) rejection be withdrawn.

2. The rejection of claim 15 is improper because the Examiner ignores claim limitations directed to the optical beam pulse length.

With particular respect to claim 15, the Section 103(a) rejection is improper because the proposed combination fails to correspond to each of the claimed limitations. Ignoring Appellant's arguments, the Examiner repeatedly concluded that "since criticality has not

been established it would be obvious to use any pulse length needed for circuit analysis as a matter of design choice." Claim 15 is specifically directed to an optical beam arrangement adapted to pulse a laser at "femto-second-range pulses," with the modulation being important for a circuit structure problem that is not a concern for the '179 reference. The import of the claimed pulse length is specifically discussed at page 7, lines 8-11: "The femto-second pulse duration aids in analysis of circuitry operating at high frequency, and in circuitry located such that analysis using a laser having a longer pulse or constant application would harm the die." The Examiner cannot ignore such specific claim limitations when none of the cited references recognize or address the problem. *See* MPEP § 2141.02. This is part of the "subject matter as a whole" which should always be considered in determining the obviousness of an invention under 35 U.S.C. § 103. Moreover, the Examiner failed to respond to these previously-presented arguments, thereby violating MPEP § 707.07(f). Without a showing of correspondence to each of the claimed limitations, the Section 103(a) rejection cannot stand and Appellant requests that the rejection be withdrawn.

VIII. Conclusion

In view of the above, Appellant submits that the rejections are improper, the claimed invention is patentable, and that the rejections of claims 12-20 should be reversed. Appellant respectfully requests reversal of the rejections as applied to the appealed claims and allowance of the entire application.

Authority to charge the assignee's deposit account was provided on the first page of this brief.

Respectfully submitted,

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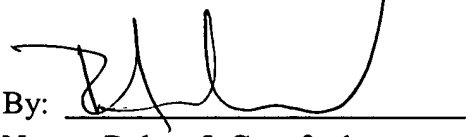
By: 

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APPENDIX OF APPEALED CLAIMS FOR APPLICATION NO. 09/932,085

12. (original) An arrangement for analyzing an integrated circuit having a silicon on insulator (SOI) structure, the arrangement comprising;

means for directing a modulated optical beam at a selected portion of the SOI structure, the modulation being adapted to inhibit optical beam intrusion upon the integrated circuit; and

means for obtaining a reflected optical waveform response from the SOI selected portion.

13. (original) A system for analyzing an integrated circuit having a silicon on insulator (SOI) structure, the system comprising;

an optical beam arrangement adapted to direct a modulated optical beam at a selected portion of the SOI structure and to inhibit intrusion of the optical beam upon the integrated circuit via the modulation; and

a detection arrangement adapted to detect a reflected optical waveform response from the SOI structure selected portion.

14. (original) The system for analyzing an integrated circuit having a silicon on insulator (SOI) structure of claim 13, wherein the optical beam arrangement includes an infrared laser.

15. (original) The system for analyzing an integrated circuit having a silicon on insulator (SOI) structure of claim 14, wherein the optical beam arrangement is adapted to pulse the laser at femto-second-range pulses.

16. (original) The system for analyzing an integrated circuit having a silicon on insulator (SOI) structure of claim 14, further comprising a testing device adapted to operate the die.

17. (original) The system for analyzing an integrated circuit having a silicon on insulator (SOI) structure of claim 13, further comprising a computer arrangement coupled to the

detector arrangement and adapted to receive and process the reflected optical waveform response.

18. (original) The system for analyzing an integrated circuit having a silicon on insulator (SOI) structure of claim 17, further comprising a visual output arrangement coupled to the computer arrangement and adapted to present data from the computer arrangement for visual analysis.

19. (original) The system for analyzing an integrated circuit having a silicon on insulator (SOI) structure of claim 18, wherein the visual output arrangement includes at least one of: a video monitor and a printer.

20. (original) The system for analyzing an integrated circuit having a silicon on insulator (SOI) structure of claim 19, wherein the computer arrangement includes waveform analysis software.

APPENDIX OF EVIDENCE FOR APPLICATION NO. 09/932,085

Appellant is unaware of any evidence submitted in this application pursuant to 37 C.F.R. §§ 1.130, 1.131, and 1.132.

APPENDIX OF RELATED PROCEEDINGS FOR APPLICATION NO. 09/932,085

As stated in Section II above, Appellant is unaware of any related appeals, interferences or judicial proceedings.